

## EE/CprE/Se 492 Weekly Report 2

1/31/25 - 2/13/25

sdmay25-28

Digital ASIC fabrication

Client & Advisor: Dr. Duwe

### Team Members

Calvin Smith – Accelerator Design lead

Camden Fergen – DevOps and Project Lead

John – Testing Lead

Nicholas – Harden and Verification lead

Levi – Communication Interfaces Lead

### Weekly Summary

Did not accomplish much this week since most members were busy, but met and have strong plans on what needs to be completed in the coming week. Have good schedule and timing so far so no delays in anything.

### Pask Week Accomplishments

- Calvin:
  - Began implementation of the top level CyGRA module for version 1.0
  - RISCv review for the sake of finding space in the ISA for various configuration and operation instructions.
  - Worked out logistics of mapping specific complex CGRA operations to single instructions independent of config
- Camden:
  - I have been sick and suffering all week
  - Looked at what needed to be done for test benches for memory controller
- John:
  - I was able to finish the testbenches for the accelerator submodule
    - PE Testbench
    - Multiplier Testbench
    - Adder Testbench
  - Started the testbench for the memory controller
  - Started writing the decoder for the CyGRA
  - Created a wrapper for the processing element array
- Levi:

- Nicholas:
  - Did research about potential on-chip memory that could replace our current solution
  - Used openRam to generate memory

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	<ul style="list-style-type: none"> <li>• Cygra implementation</li> <li>• RISCv research</li> <li>• State machine instruction mapping</li> </ul>	8	90.044
Camden	<ul style="list-style-type: none"> <li>• Got acquainted with memory controller</li> <li>• Prepared to write test benches</li> </ul>	4	72
John	<ul style="list-style-type: none"> <li>• Multiple testbenches</li> <li>• CyGRA decoder</li> <li>• PE array wrapper</li> </ul>	16	88
Levi			68
Nicholas	<ul style="list-style-type: none"> <li>• Memory research</li> <li>• Memory synthesis</li> </ul>	6	96

#### Plans for Upcoming Week

- Calvin:
  - Finish CyGRA v1.0 implementation
  - Present Minimum viable product for synthesis and hardening
  - Begin CyDMA/CyGRA v1.1 work
- Camden:
  - Complete stuff i didnt get done last week (test benches)
  - Continue to scrum

John:

- Levi:
- Nicholas:

#### Summary of weekly advisor meeting

Met with Duwe but did not have much to present. Got some feedback from him on a few aspects of the design. Advised us to ensure we have good time planning since workload will increase as we get closer to efabless submission date.